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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/041,092	12/28/2001	James S. Burns	42390P12492	2392

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EXAMINER

CHEN, TSE W

ART UNIT	PAPER NUMBER
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2116

DATE MAILED: 11/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/041,092

Applicant(s)

BURNS ET AL.

Examiner

Tse Chen

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 December 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 331,814,1020,1114.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on March 31, 2003, August 14, 2003, October 20, 2003, and November 14, 2003, were filed before the mailing date of the first Office Action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

2. The disclosure is objected to because of the missing Brief Summary of the Invention. See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention. Appropriate correction is required.

3. The disclosure is objected to because of the following informalities: the related US Patent Application number 10041013 for "Multiple Mode Digital Throttle Mechanism" should be filled in on page 2. Appropriate correction is required.

4. Claims 1, 26 and 28 are objected to because of the following informalities:

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- As per claim 1, “operating state” does not correspond to the antecedent “operating point” established on line 4 of claim 1.
- As per claim 26, “further comprising” should be “further comprises”.
- As per claim 28, “activate” should be “active”.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 6, 19, 20, 25-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Soltis, Jr. et al., US Patent 6651176, hereinafter Soltis.

7. In re claim 1, Soltis discloses a system [100] comprising:

- An execution pipeline [116].
- A power delivery unit [inherently, a power delivery unit in the broadest interpretation is needed to provide power] to provide power to the execution pipeline at a specified operating state [col.4, ll.40-56; col.5, l.66 – col.6, l.62; col.7, ll.14-56; full or low power state as related to bleed rate].
- A digital throttle [power dissipation controller 118] to estimate a power state [capacity 322], responsive to activity of the execution pipeline and the specified operating state, and to trigger a change in the operating state, responsive to the estimated power state

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reaching a first threshold [363] [col.4, ll.9-17, ll.40-56; col.5, l.66 – col.6, l.62; col.7, ll.14-56; col.8, ll.25-36; switch to low power state if capacity as determined by first power dissipation at full power state exceeds threshold].

8. In re claim 6, Soltis discloses each and every limitation of the claim as discussed above in reference to claim 1. Additionally, Soltis discloses a gate unit to indicate an activity state for the one or more units [col.6, ll.16-62; tagging of lp-bits].

9. In re claim 19, Soltis discloses each and every limitation of the claim as discussed above in reference to claim 1. Additionally, Soltis discloses monitoring activity states for pipeline units of the processor [col.2, l.66 – col.3, l.40; col.4, ll.9-67].

10. As to claim 20, Soltis discloses each and every limitation of the claim as discussed above in reference to claim 19. Additionally, Soltis discloses normalizing the scaled activity level relative to a first threshold and accumulating the normalized, scaled activity level for a series of clock intervals [col.2, l.66 – col.3, l.40; col.4, ll.9-67; fig.8; normalizing to target].

11. As to claim 25, Soltis discloses the method wherein estimating the activity level comprises adding a first or a second weight value to a sum, responsive to a pipeline unit being in a first or a second activity state, respectively and scaling the sum by a factor associated with the current operating point [col.2, l.66 – col.3, l.40; col.4, ll.9-67; col.7, l.14 – col.8, l.47].

12. As to claim 26, Soltis discloses the method wherein estimating the activity level comprises adding a weight to the sum to represent pipeline units that operate in a single activity state [col.2, l.66 – col.3, l.40].

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13. In re claim 27, Soltis discloses each and every limitation of the claim as discussed above in reference to claim 19. Additionally, Soltis discloses a memory system to store instructions for execution [instruction cache 114].

14. As to claim 28, Soltis discloses the computer system wherein the power delivery system includes plural gate units, each gate unit to indicate a first or second activity state for a unit of the execution pipeline, according to the unit's being active or inactive in a clock interval [col.6, ll.16-62; tagging of lp-bits].

15. As to claims 29 and 30, Soltis discloses each and every limitation as discussed above in reference to claim 25.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

17. Claims 2-3, 11-15, 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soltis as applied to claim 1 above, and further in view of Huang et al., US Patent 6407595, hereinafter Huang.

18. In re claim 2, Soltis discloses each and every limitation of the claim as discussed above in reference to claim 1. In particular, Soltis discloses the system that includes a clock gating circuit [inherently, some clock gating circuit in the broadest interpretation is needed to control clock capacity with the lp-bits] to control power delivery to one or more units of the execution pipeline

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[col.2, 1.66 – col.3, 1.40; col.4, 11.9-67; clock capacity related to 1p-bits]. Soltis did not disclose explicitly that the power delivery unit includes the clock gating circuit to control power delivery.

19. Huang discloses a system wherein the power delivery unit [fig.1] includes a clock gating circuit [13] to control power delivery [col.2, 1.34 – col.3, 1.16].

20. It would have been obvious to one of ordinary skill in the art, having the teachings of Soltis and Huang before him at the time the invention was made, to use the power delivery unit taught by Huang for the system disclosed by Soltis in order to provide the system wherein the power delivery unit includes a clock gating circuit to control power delivery to one or more units of the execution pipeline. One of ordinary skill in the art would have been motivated to make such a combination as it provides an efficient way to control processing temperature in a digital system [Huang: col.1, 1.10 – col.2, 1.10].

21. As to claim 3, Soltis discloses the system wherein the digital throttle comprises an activity monitor to estimate an activity level [first power dissipation] responsive to a signal [valid instructions] from the clock gating circuit, the activity monitor including a scaling unit [issue weight] to adjust the estimated activity level, responsive to the current operating state [col.2, 1.66 – col.3, 1.40; col.4, 11.9-67].

22. In re claim 11, Soltis and Huang discloses each and every limitation of the claim as discussed above in reference to claims 1-3.

23. As to claim 12, Soltis discloses the processor wherein the scaling unit includes a look-up table [119] and a multiplier, the look-up table to provide a scale factor [constants; i.e., weights] [col.4, 11.57-67] to the multiplier, responsive to the operating point of the processor [col.4, 11.9-25].

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24. As to claim 13, the Examiner hereby takes Official Notice that it is well known in the art to specify an operating state [e.g., low or full power] by a voltage and a frequency [decreasing clock frequency decreases power consumption].

25. As to claim 14, the Examiner hereby takes Official Notice that it is well known in the art to increment values [e.g., comparative differences] in an accumulator.

26. As to claim 15, the Examiner hereby takes Official Notice that it is well known in the art to have multiple threshold comparisons in order to transition to different states.

27. As to claim 22, Soltis and Huang disclose each and every limitation of the claim as discussed above in reference to claim 2.

28. As to claims 23-24, Soltis discloses the method wherein adjusting the operating point of the processor comprises adjusting a frequency and voltage of the clock signal [col.2, l.66—col.3, l.40].

29. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Soltis and Huang as applied to claim 3 above, and further in view of Dunstan et al., US Patent 5694607, hereinafter Dunstan.

30. Soltis and Huang disclose each and every limitation of the claim as discussed above in reference to claim 3. In particular, Soltis discloses the system wherein the scaling unit includes a look-up talbe [119] to store scaling factors [constants; i.e., weights] [col.4, ll.57-67] and a multiplier to multiply the estimated activity level by the scaling factor associated with the current operating point [col.4, ll.9-25]. Soltis and Huang did not discuss multiple operating states.

31. Dunstan discloses a look-up table [70] to store values for a plurality of operating states [configurations] [col.7, ll.39-65].

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32. It would have been obvious to one of ordinary skill in the art, having the teachings of Dunstan, Soltis and Huang before him at the time the invention was made, to use the look-up table taught by Dunstan for the system disclosed by Soltis and Huang in order to provide the system wherein the scaling unit includes a look-up table to store scaling factors for a plurality of operating points. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to track and control power consumption in a multiple operating state system [Dunstan: col.1, 1.9 – col.2, 1.51].

33. Claims 5 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soltis and Huang as applied to claims 3 and 11 above, and further in view of Niegel et al., US Patent 6512757, hereinafter Niegel.

34. In re claim 5, Soltis and Huang disclose each and every limitation of the claim as discussed above in reference to claim 3. Soltis did not discuss weight units associated with the units of the pipeline.

35. Niegel discloses a system wherein a monitor unit comprises a plurality of weight units, each weight unit being associated with one of the units of execution pipeline and an adder to receive a first or second value from each weight unit [col.2, 1.57 – col.2, 1.31].

36. It would have been obvious to one of ordinary skill in the art, having the teachings of Niegel, Soltis and Huang before him at the time the invention was made, to use the weight units taught by Niegel for the system disclosed by Soltis and Huang in order to provide the system wherein the monitor unit comprises a plurality of weight units, each weight unit being associated with one of the units of the execution pipeline and an adder to receive a first or second value from each weight unit, responsive to the signal from the clock gating circuit.. One of ordinary

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skill in the art would have been motivated to make such a combination as it provides a way to process a plurality of data channels at reduced hardware costs, while maintaining a high processing speed and short time delay [Niegel: col.1, 1.13 – col.2, 1.41].

37. As to claim 16, Niegel, Soltis and Huang disclose each and every limitation of the claim as discussed above in reference to claim 5.

38. As to claim 17, Niegel, Soltis and Huang disclose each and every limitation of the claim as discussed above in reference to claim 16. Niegel, Soltis and Huang did not disclose explicitly monitoring status signals provided by the gate units.

39. It would have been obvious to one with ordinary skill in the art to monitor the activity states by monitoring the status signals provided by gate units associated with the pipeline units of the processor as the monitoring of the status signals is well-known in the art and suitable for use in the system disclosed by Niegel, Soltis and Huang. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to gauge the status of activity in the pipeline.

40. As to claim 18, Niegel, Soltis and Huang disclose each and every limitation of the claim as discussed above in reference to claims 16 and 17.

41. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soltis as applied to claim 1 above, and further in view of Dunstan.

42. In re claim 7, Soltis discloses each and every limitation of the claim as discussed above in reference to claim 3. In particular, Soltis discloses the system wherein the scaling unit includes a look-up talbe [119] to store scaling factors [constants; i.e., weights] [col.4, ll.57-67] and a

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multiplier to multiply the estimated activity level by the scaling factor associated with the current operating point [col.4, ll.9-25]. Soltis did not discuss multiple operating states.

43. Dunstan discloses a look-up table [70] to store values for a plurality of operating states [configurations] [col.7, ll.39-65].

44. It would have been obvious to one of ordinary skill in the art, having the teachings of Dunstan and Soltis before him at the time the invention was made, to use the look-up table taught by Dunstan for the system disclosed by Soltis in order to provide the system wherein the scaling unit includes a look-up table to store scaling factors for a plurality of operating points. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to track and control power consumption in a multiple operating state system [Dunstan: col.1, l.9 – col.2, l.51].

45. As to claim 8, Soltis discloses the system comprising a conversion circuit [part of 118] to determine a power state [capacity] from the adjusted activity level [col.4, ll.9-17, ll.40-56; col.5, l.66 – col.6, l.62; col.7, ll.14-56; col.8, ll.25-36].

46. As to claim 9, the Examiner hereby takes Official Notice that it is well known in the art to store values [e.g., comparative differences] in an accumulator.

47. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dunstan and Soltis as applied to claim 9 above, and further in view of Yochai et al., US Patent 6721870, hereinafter Yochai.

48. Dunstan and Soltis disclose each and every limitation of the claim as discussed above in reference to claim 9. Dunstan and Soltis did not discuss scaling the threshold level.

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49. Yochai discloses a system wherein a conversion unit scales the threshold level responsive to the current operating point [col.9, 1.65 – col.10, 1.50].

50. It would have been obvious to one of ordinary skill in the art, having the teachings of Yochai, Dunstan and Soltis before him at the time the invention was made, to use the conversion unit taught by Yochai for the system disclosed by Dunstan and Soltis in order to provide the system wherein the conversion unit scales the threshold level responsive to the current operating point. One of ordinary skill in the art would have been motivated to make such a combination as it provides an efficient way to prefetch instructions or data [Yochai: col.1, 1.27 – col.2, 1.11].

51. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Soltis as applied to claim 19 above.

52. Soltis discloses each and every limitation of the claim as discussed above in reference to claim 19. Soltis did not disclose explicitly monitoring status signals provided by the gate units.

53. It would have been obvious to one with ordinary skill in the art to monitor the activity states by monitoring the status signals provided by gate units associated with the pipeline units of the processor as the monitoring of the status signals is well-known in the art and suitable for use in the system disclosed by Soltis. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to gauge the status of activity in the pipeline.

Conclusion

54. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited U.S. patent documents describe various methods, systems, and well-known attributes associated with pipeline processing and related arts.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
November 17, 2004



REHANA PERVEEN
PRIMARY EXAMINER